IN THE CLAIMS

1. (Currently amended) A method of operating a memory at a maximum rate, comprising:

initiating a first memory operation;

identifying a completion of the first memory operation;

generating a cycle ready strobe signal upon the identified completion; [[and]]

employing the cycle ready strobe signal for initiation of a next memory operation;

wherein initiating the first memory operation or initiating the next memory operation comprises:

triggering a transition of an internal memory clock signal;

transitioning a bit line precharge signal to disable a bit line precharge operation based on the transition of the internal memory clock signal;

enabling selected row and column decoder circuitry for addressing one or more selected memory cells within the memory based on the transition of the internal memory clock signal;

initiating a tracking circuit that waits a predetermined tracking time associated with a time needed for selected true and complementary bit lines associated with the one or more selected memory cells to establish a voltage differential therebetween based on a state of the one ore more selected memory

cells, the initiation of the tracking circuit based on the transition of the internal memory clock signal; and

outputting a reset signal from the tracking circuit after the predetermined tracking time, thereby disabling the internal memory clock signal, and initiating a bit line precharge operation.

2. (Original) The method of claim 1, wherein the memory operation comprises a read operation.

3. (Original) The method of claim 1, wherein initiating a memory operation comprises:

inputting a clock strobe signal associated with a system clock signal into a memory control circuit operable to generate one or more memory control signals upon receipt of the clock strobe signal.

4. (Original) The method of claim 3, wherein one of the control signals comprises a bit line precharge enable signal, and wherein generating the cycle ready strobe signal comprises activating a cycle ready circuit when the bit line precharge enable signal transition to indicate initiation of a bit line precharge operation.

5. (Original) The method of claim 4, wherein activating the cycle ready circuit causes the cycle ready circuit to

generate the cycle ready strobe signal a predetermined time after the bit line precharge enable signal transition.

6. (Original) The method of claim 5, wherein the predetermined time is sufficient to ensure that one or more true and complement bit line pairs substantially equalize and reach a predetermined precharge level.

7. (Original) The method of claim 6, wherein the predetermined time varies with respect to at least one of voltage, temperature and process condition variations.

8. (Original) The method of claim 7, wherein the variation in the predetermined time correlates substantially with a variation in time for the one or more true and complement bit line pairs substantially equalize and reach the predetermined precharge level due to variations in one or more of voltage, temperature and process conditions.

9. (Original) The method of claim 1, wherein employing the cycle ready strobe signal for initiation of the next memory operation comprises:

identifying the generation of the cycle ready strobe signal;

modifying a multiplexer input select control signal in response thereto;

feeding a memory multiplexer logic circuit with both the clock strobe signal and the cycle ready strobe signal; and

using the modified multiplexer input select control signal to pass the cycle ready strobe signal to a memory control circuit to generate one or more memory control signals for initiating the next memory operation.

10. (Original) The method of claim 1, wherein identifying the completion of the memory operation comprises detecting a bit line precharge enable signal transition indicating an initiation of a bit line precharge process.

11. (Currently amended) A method of operating a memory, comprising:

initiating a first memory operation with an input clock signal associated with a system clock;

generating a cycle ready strobe signal upon a completion of the memory operation; [[and]]

using the cycle ready strobe signal to initiate a next memory operation;

wherein initiating the first memory operation or initiating the next memory operation comprises:

triggering a transition of an internal memory clock signal;

transitioning a bit line precharge signal to disable a bit line precharge operation based on the transition of the internal memory clock signal;

enabling selected row and column decoder circuitry for addressing one or more selected memory cells within the memory based on the transition of the internal memory clock signal;

initiating a tracking circuit that waits a predetermined tracking time associated with a time needed for selected true and complementary bit lines associated with the one or more selected memory cells to establish a voltage differential therebetween based on a state of the one ore more selected memory cells, the initiation of the tracking circuit based on the transition of the internal memory clock signal; and

outputting a reset signal from the tracking circuit after the predetermined tracking time, thereby disabling the internal memory clock signal, and initiating a bit line precharge operation.

12. (Original) The method of claim 11, wherein the cycle ready strobe signal transitions to enable initiation of the next memory operation a predetermined period of time after the completion of the memory operation.

13. (Original) The method of claim 12, further comprising identifying the completion of the memory operation by identifying a transition of a bit line precharge enable signal, wherein the

transition indicates an initiation of a bit line precharge process.

14. (Original) The method of claim 13, wherein the predetermined period of time is sufficient to ensure that one or more true and complement bit line pairs substantially equalize and reach a predetermined precharge level.

15. (Original) The method of claim 14, wherein the predetermined time period varies with respect to at least one of voltage, temperature and process condition variations.

16. (Original) The method of claim 15, wherein the variation in the predetermined time period correlates substantially with a variation in time for the one or more true and complement bit line pairs substantially equalize and reach the predetermined precharge level due to variations in one or more of voltage, temperature and process conditions.

17. (Cancelled)